A Low-Cost-Packaged 4.9-6 GHz LNA for WLAN Applications

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Abstract — **A two stage fully integrated low-noise amplifier has been developed for 4.9-6GHz WLAN applications. This circuit was realized in 0.35µm SiGe BICMOS process and packaged in low cost plastic VFQFPN package. The circuit operates over a wide band (4.9-6GHz) and draws 13.2mA from 2.0V supply. It exhibits a noise figure of 3.9dB and a gain of 18.7dB at 5.5GHz. The measured IIP1 and IIP3 are respectively –13.9dBm and -3.5dBm at 5.5GHz. The input and output return losses are lower than –10dB and the gain ripple is less than 1.5dB all over the frequency bandwidth.**

I. Introduction

The trend towards interactive multimedia services has driven the development of new wireless systems with increased bandwidth. Next generation Wireless Local Area Network (WLAN) operates at various frequencies in the 5-6 GHz bandwidth. In commercial and consumer applications cost must be kept low, therefore low cost package and a foundry process with proven yield and reliability must be used. 5GHz WLAN systems require low cost wideband Low Noise Amplifier (LNA) to cover the allocated frequency bands of the different standards in US (IEEE 802.11a), Europe (ETSI BRAN Hiperlan/2), and Japan (MMAC HiSWANa), that is to say from 4.9 GHz to 5.825 GHz.

Numerous C-band LNA designs have been presented in different technologies: MESFET [1]-[3], SiGe HBT [4], SiGe BiCMOS [5]-[6], CMOS [7]. Although some LNAs exhibit better noise figure [1]-[6], or lower DC power consumption [1]-[4],[6], the results of the LNA presented hereafter are the first results to our knowledge in a 20-pin leadless plastic package of a wideband (4.9-6GHz), fully integrated (on chip matching networks) single-ended circuit. This LNA features a noise figure of 3.9dB, a gain of 18.7dB, IIP1 of –13.9dBm and a IIP3 of –3.5dBm at 5.5GHz. The input and output return losses are lower than –10dB from 4.9GHz up to 6GHz. Moreover, this circuit response is quite flat over 4.9-6 GHz: the gain ripple is only 1.4dB.

II. Circuit Design

The LNA circuit was designed to be packaged in a leadless plastic package and to be fully matched on chip, without any external reactive elements. In order to reduce silicon area, a single-ended topology was chosen, but this choice causes a more difficult accurate assessment of the ground paths.

Figure 1 gives a simplified schematic of the LNA chip. The designed LNA is composed of two stages with inductive emitter degeneration, partly realized with down-bonding wires to the package die pad. The first stage is optimized for noise figure performance and the second one for gain. The ground path is separated between the two stages for stability purpose. The transistor size of the first stage is selected to be 0.35 x 3x 10 μm^2, which enables an easier trade-off between 50 Ohm input matching and noise figure performance. The second stage transistor has the same size.

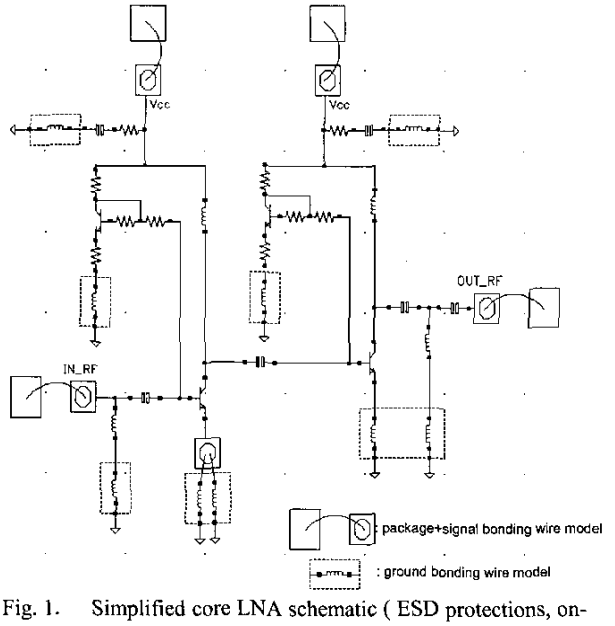

Fig. 1. Simplified core LNA schematic (ESD protections, on-chip metal interconnection models are not indicated).

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During simulation phase, accurate models are necessary for active and passive devices. Within the frequency range of our interest, metal interconnections, bonding wires and package have to be imperatively modeled and taken into account from the beginning of simulations. The impedance of the ground paths has not to be neglected due to the single-ended architecture of the circuit.

The input and output matching networks are fully integrated on chip. The parasitic elements of the package and the bonding wire inductances are taken into account in the matching network synthesis in order to avoid frequency shift at the package accesses. To reduce the ground inductances, the number of ground bonding wires (wires connecting the die and the leads, wires connecting the die and the metallic die paddle) was optimized.

As the LNA is packaged, electrostatic discharge (ESD) protections are implemented. Indeed, as RF applications are sensitive to parasitic component influence, the best ESD protection approach is the use of an association of ESD diodes and power clamp protection scheme [8].

III. Realization / Implementation

A. BICMOS Process [9]

The LNA was realized in a production 200mm 0.35µm SiGe BiCMOS process from STMicroelectronics. The technology is characterized by the choice of simple, manufacturable process options, such as conventional LOCOS isolation, non selective Si/SiGe epitaxy and the use of quasi self aligned E/B structure. A selective implanted collector allows two types of transistors on the same chip, with typical 45 and 25GHz transit frequency, and respectively 60 and 50GHz maximum frequency of oscillation. Furthermore, this process features 5 level metal interconnections, and the latter is a thick Al-Cu layer. Several types of resistors, metal-insulator-metal capacitors, and inductors are available.

The chip size of the LNA is 1.65 x 1.13mm^2 including pads, ESD protections. Figure 2 shows a microphotograph of the LNA chip.

B. Package and test board

The selected package is a Very Fine pitch Quad Flat Package Non leaded (VFQFPN, normalized by JEDEC) which presents the advantage of an exposed metallic die paddle backside contact for good thermal and electrical performance. The size of the selected one is 4 x 4 mm^2, with a cavity of 2.3 x 2.3 mm^2, and the number of leads is 20, five leads at each side. The package is then welded on a test board (each lead and the die paddle are welded).

A layout view of the test board is presented in Figure 3. The substrate of the test board is a 2 metal layer ROGERS 4350 with a relative dielectric constant of 3.48 and a thickness of 0.8mm.

The RF input and output accesses are realized with 50 Ohm characteristic impedance lines. The gap between these transmission lines and the top layer ground plates is large enough to enable microstrip propagation. The top and bottom ground plates are connected by a high number of via holes to achieve the modeled transmission line performance. For the DC supply, 50 Ohm characteristic impedance line is also used, and two RC filters and capacitors have been added to decouple and filter spurious signals due to the DC generator.

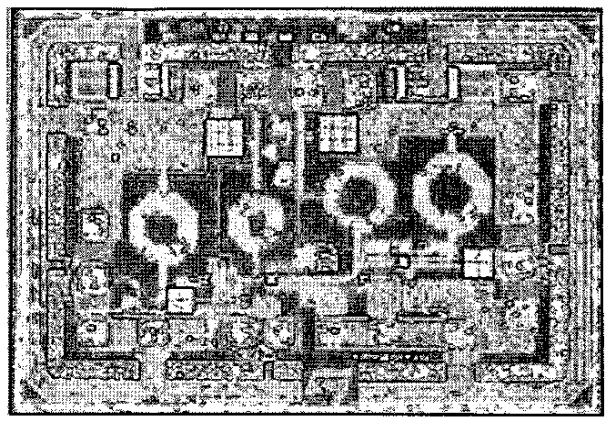

Fig. 2. Chip microphotograph.

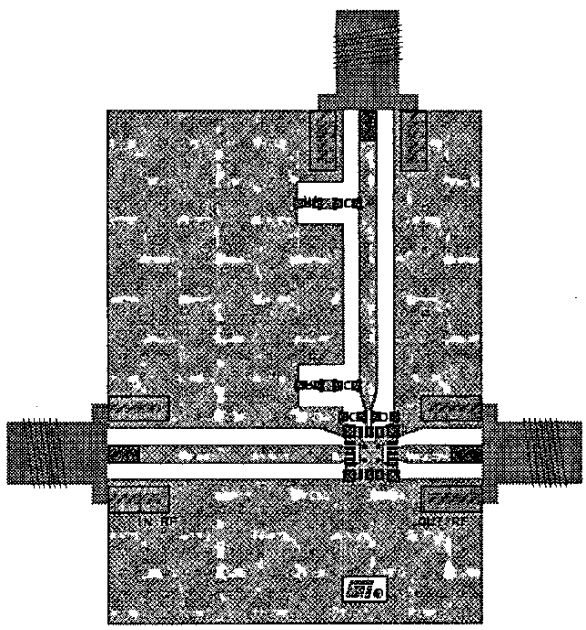

Fig. 3. Test board layout view.

IV. MEASURED RESULTS

The packaged LNA scattering parameters and noise figure were measured from 4 GHz to 7 GHz. The LNA draws 13.2mA from a 2V supply. The measured gain and noise figure for Vcc=2V are shown in Fig. 4. The ripple gain over 4.9 GHz - 6 GHz is about 1.5 dB, and its value at 5.5 GHz is 18.7dB. The noise figure at 5.5 GHz is about 3.9dB, but it is maximum at 6 GHz (4.2dB).

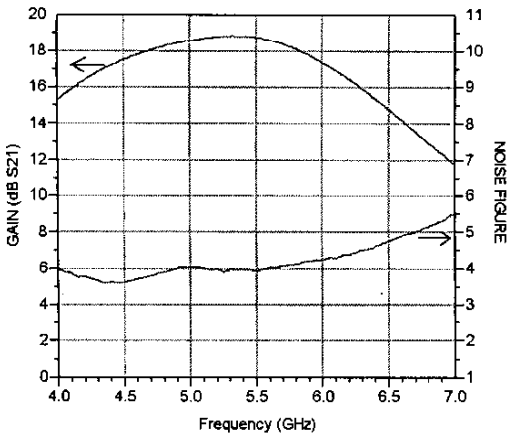

Fig. 4. Measured S21 and noise figure at 2V, 25^{0}C

The input and output VSWR are presented respectively in figures 5 and 6.

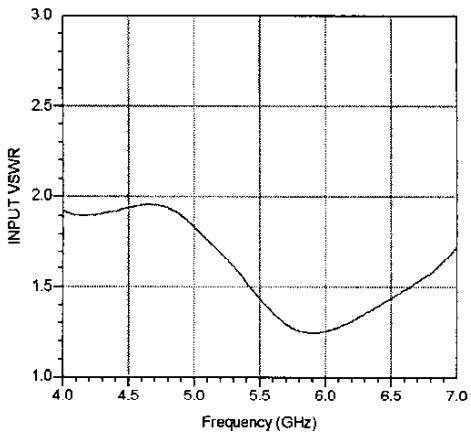

Fig. 5. Measured input VSWR at 2V, 25^{0}C

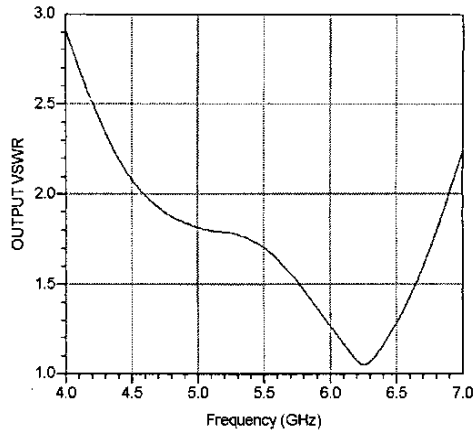

Fig. 6. Measured output VSWR at 2V, 25^{0}C

Another important feature of a LNA circuit is its non-linear behavior. The compression gain of the LNA is measured at 5.5GHz; the characteristic output power versus input power is presented Fig.7.

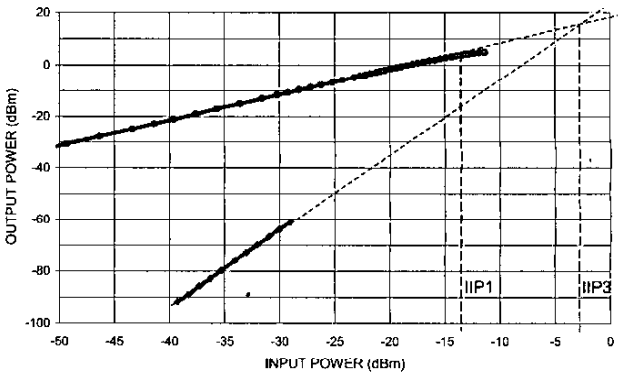

Fig. 7. Measured gain compression at 2V, 25^{0}C

The measured input referred 1dB compression point (IIP1) is –13.9dBm.

The linearity of the LNA is also measured by applying two RF signals at frequencies f_1=5.4915GHz and f_2=5.5085GHz and measuring the power levels of the third-order intermodulation product at $2f_2$-f_1 and $2f_1$-f_2. The measured input third-order intermodulation intercept (IIP3) is –3.5dBm.

Table 1 summarizes the measurement results of the LNA from 5.15 GHz to 5.825 GHz.

TABLE I
SUMMARY OF LNA MEASURED CHARACTERISTICS

	Min value	Max value	Unit
Frequency	5.15	5.825	GHz
Gain	17.95	18.82	dB
NF	3.9	4.2	dB
Input VSWR	1.25	1.73	-
Output VSWR	1.42	1.79	-
Supply @2V	13.2		mA
IIP1 @5.5GHz	-13.9		dBm
IIP3	-3.5 @ Δf=17MHz		dBm

V. CONCLUSION

A 4.9 - 6 GHz LNA, implemented in a 0.35µm SiGe BICMOS technology and packaged in a low-cost plastic package was reported. Over the frequency range, the measured gain is higher than 17dB, the noise figure is less than 4.2dB, and the input and output matching are lower than –10dB, and the gain ripple is lower than 1.5dB. The 1dB gain compression point is –13.9dBm @ 5.5 GHz. These results demonstrate the feasibility of low-cost single-ended circuits at 6 GHz, assembled in a low cost plastic package for wireless communication systems.

ACKNOWLEDGEMENTS

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